What is claimed is:

1. A method of forming a via plug, the method comprising:

directing an aerosol stream of particles of a conductive material into a via of an integrated circuit device to deposit the conductive material within the via.

2. The method of claim 1, wherein the via is disposed in a substrate or in a dielectric layer disposed on a base layer of the integrated circuit device.

3. The method of claim 2, wherein the base layer is a metal layer or an active area of the integrated circuit device.

4. The method of claim 1, further comprising liquefying the particles by passing the aerosol stream through a laser beam before the conductive material is deposited in the via.

5. The method of claim 1, further comprising while the particles are in the via, sintering the particles.

6. The method of claim 5, wherein sintering the particles comprises using a laser or heating the particles and the integrated circuit device in an oven.

7. The method of claim 1, further comprising covering an end of the via while the aerosol steam passes through an opposite end of the via.

8. The method of claim 1, wherein directing an aerosol stream of particles of a conductive material into a via comprises directing the aerosol steam on a sidewall of the via for coating the sidewall to form a hollow via plug.

9. The method of claim 1, wherein the particles of the conductive material are nano-particles.

10. The method of claim 1, wherein the via is a blind-hole via that terminates at a base layer or a through-hole via that passes completely through a substrate.

11. The method of claim 1, wherein the conductive material is a silver-based material.

12. A method of forming a via plug, the method comprising:

directing an aerosol stream of particles of a first conductive material onto a sidewall of a via disposed in a substrate or in a dielectric layer disposed on a base layer of an integrated circuit device to form a seed layer of the first conductive material on the sidewall; and

plating the seed layer with a second conductive material.

13. The method of claim 12, wherein plating the seed layer with a second conductive material comprises plating the seed layer with a second conductive material that is substantially the same as the first conductive material.

14. The method of claim 12, wherein plating the seed layer with the second conductive material comprises electroplating or electrolessly plating the seed layer with the second conductive material.

15. The method of claim 12, further comprising before plating the seed layer, aggregating the particles of the first conductive material to form a coherent mass of the first conductive material on the sidewall.

16. The method of claim 12, wherein the first conductive material is silver and the second conductive material is copper.

17. A method of forming an integrated circuit device, the method comprising:
forming a dielectric layer on a base layer of the integrated circuit device;
forming a via in the dielectric layer terminating at the base layer; and
forming a via plug within the via by directing an aerosol stream of particles of a conductive material into the via to deposit the conductive material within the via contacting the base layer.

18. The method of claim 17, further comprising aggregating the particles before or after depositing the conductive material within the via.

19. The method of claim 17, further comprising forming a metal layer on the dielectric layer in contact with the via plug so that the via plug interconnects the metal layer and the base layer.

20. The method of claim 17, wherein the base layer comprises integrated circuit elements.

21. The method of claim 17, wherein directing an aerosol stream of particles of a conductive material into a via comprises directing the aerosol steam on a sidewall of the via for coating the sidewall to form a hollow via plug.

22. A method of forming an integrated circuit device, the method comprising:
forming a dielectric layer on a base layer of the integrated circuit device;
forming a via in the dielectric layer terminating at the base layer; and
forming a via plug within the via, wherein forming the via plug comprises:
directing an aerosol stream of particles of a first conductive material onto a sidewall of the via to form a seed layer of the first conductive material on the sidewall; and
plating the seed layer with a second conductive material.

23. The method of claim 22, further comprising before plating the seed layer, aggregating the particles of the first conductive material to form a coherent mass of the first conductive material on the sidewall.

24. The method of claim 22, wherein plating the seed layer with a second conductive material comprises plating the seed layer with a second conductive material that is substantially the same as the first conductive material.

25. The method of claim 22, further comprising forming a metal layer on the dielectric layer in contact with the via plug so that the via plug interconnects the metal layer and the base layer.

26. A method of manufacturing an integrated memory circuit, wherein the memory circuit comprises an array of memory cells connected to column and row address decoders and a sensing circuit, the method comprising:

forming a via plug in the memory circuit by directing an aerosol stream of particles of a conductive material into a via of the memory circuit to deposit the conductive material within the via.

27. The method of claim 26, further comprising, before forming the via plug:

forming a dielectric layer on a base layer of the memory circuit; and

forming the via in the dielectric layer.

28. The method of claim 27, further comprising forming a metal layer on the dielectric layer in contact with the via plug so that the via plug interconnects the metal layer and the base layer.

29. The method of claim 26, further comprising aggregating the particles before or after depositing the conductive material within the via.

30. A method of manufacturing an integrated memory circuit, wherein the memory circuit comprises an array of memory cells connected to column and row address decoders and a sensing circuit, the method comprising:

forming a via plug in the memory circuit, wherein forming the via plug comprises:

directing an aerosol stream of particles of a first conductive material onto a sidewall of a via of the memory circuit to deposit the conductive material within the via form a seed layer of the first conductive material on the sidewall; and

plating the seed layer with a second conductive material.

31. The method of claim 30, further comprising before plating the seed layer, aggregating the particles of the first conductive material to form a coherent mass of the first conductive material on the sidewall.

32. The method of claim 30, wherein plating the seed layer with a second conductive material comprises plating the seed layer with a second conductive material that is substantially the same as the first conductive material.

33. The method of claim 30, further comprising, before forming the via plug:
forming a dielectric layer on a base layer of the memory circuit; and
forming the via in the dielectric layer.

34. The method of claim 33, further comprising forming a metal layer on the dielectric layer in contact with the via plug so that the via plug interconnects the metal layer and the base layer.